Start

Is next instruction in IBR?

Yes — No memory access required

No — MAR ← PC

MBR ← M(MAR)

Left instruction required?

No — IR ← IBR (20:27) / MAR ← IBR (28:39)

Yes — IBR ← MBR (20:39) / IR ← MBR (0:7) / MAR ← MBR (8:19)

IR ← IBR (0:7) / MAR ← IBR (8:19)

PC ← PC + 1

Fetch cycle

Decode instruction in IR

Execution cycle

AC ← M(X)

Go to M(X, 0:19)

If AC > 0 then go to M(X, 0:19)

Is AC > 0? — Yes

AC ← AC + M(X)

MBR ← M(MAR)

AC ← MBR

PC ← MAR

MBR ← M(MAR)

AC ← AC + MBR

M(X) = contents of memory location whose address is X
(i:j) = bits i through j

Figure 2.4 Partial Flowchart of IAS Operation